SPECIFICATION

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HIGH IMPEDANCE ANTIFUSE

Background of the Invention

[0001] Technical Field

[0002] The invention relates generally to semiconductor integrated circuits, and more particularly to antifuse elements.

[0003] Background Art

[0004] In the field of semiconductor integrated circuits, it is generally known to construct fuse elements that can be programmed (either optically or electrically) to provide an electrical open circuit in a link that normally provides a conductive path when activated. Such elements are used for example to set a sequence of address bits for a redundant line of memory cells, or to set product information that is subsequently read when a system is first powered up.

[0005] It is also known to provide an "antifuse," which is a programmable element that provides a selective short circuit. This is typically done by providing a stimulus that decreases the resistance of a programmed element. See for example U.S. Patent 5,242,851, "Programmable Interconnect Device and Method of Manufacturing Same," which teaches the use of a line of intrinsic polysilicon that decreases in resistance from 10G ohms to 500 to 100 ohms when programmed. In U.S. Patent 5,557,136, "Programmable Interconnect Structures and Programmable Integrated Circuits," two titanium-tungsten layers are separated by amorphous silicon, which breaks down during programming to form a conductive filament where it is thinned. Selective silicide formation as an antifuse is taught in U.S. Patent 6,051,851, "Semiconductor Devices utilizing Silicide Reaction." Conductor-filled vias as a programming element are taught in Re. 36,893, "Anti-Fuse Structure For Reducing Contamination of the Anti-Fuse Material."

[0006] A particular type of antifuse that has been used more recently is the "insulator antifuse," in

which reliance is placed on dielectric breakdown of an insulator between conductors to provide the decreased resistance. U.S. Patent 5,909,049, "Antifuse Programmed PROM Cell," discloses a composite insulator of oxide, oxide-nitride, oxide (or O-N-O) that breaks down at an applied voltage of 10-18 volts to program the cell by melting the silicon below the insulator. U.S. Patent 6,020,777, "Electrically Programmable Antifuse Circuit," teaches a MOS capacitor that is programmed by Fowler-Nordheim tunneling current when the applied voltage is 2X Vdd.

[0007] All of the above teachings rely on high programming voltages or currents to substantially alter the physical or electrical properties of the programmed element. With increasing device integration, applying these high stresses to elements to be programmed increases the possibilities of damaging non-programmed circuit elements. For example, a programming voltage of 18 volts will impart electrical fields that will damage other integrated circuit elements in adjacent circuits. At the same time, it is important for the antifuse to undergo a large resistance change so that it can be reliably sensed.

[0008] Accordingly, a need has developed in the art for antifuses that can be programmed at lower applied programming energies, while still creating an indication of its programmed state.

Brief Summary of the Invention

[0009] It is thus an object of the present invention to provide antifuses that can be programmed at voltages and currents that reduce the possibility of damaging non-programmed circuit elements.

[0010] It is another aspect of the invention to provide antifuses that can be programmed at such lower applied energies while still being reliably sensed.

[0011] In a first aspect, the invention is a programmable element that has a first device having a first electrode and a first insulator disposed between the substrate and said electrode, said first insulator having a first value of a given parameter, and a second device having a second electrode and a second insulator disposed between the substrate and said second electrode, said second insulator having a second value of said given parameter that is different from said first value. The first and second electrodes are coupled to one another, and a source of programming energy is coupled to the first device to cause it to permanently decrease in resistivity when programmed. The programmed state of the first device is indicated by a conductive state of the second device.

[0013] In a third aspect, the invention is a method of forming an integrated circuit including a programmable element, comprising the steps of forming a first device on a substrate having a first electrode and a first insulator disposed between the substrate and said first electrode, the first insulator having a first value of a given parameter; forming a second device on a substrate having a second electrode and a second insulator disposed between the substrate and the second electrode, the second insulator having a second value of the given parameter that is different from the first value; coupling the first and second electrodes to one another; and coupling a source of programming energy to the first device.

Brief Description of the Several Views of the Drawings

[0014] The foregoing and other features of the invention will become more apparent upon review of the detailed description of the invention as rendered below. In the description to follow, reference will be made to the several figures of the accompanying Drawing, in which:

[0015] Fig. 1A is a cross-sectional view of the programmable element AF in accordance with a first embodiment of the invention;

[0016] Fig. 1B is a top view of Fig. 1A, in accordance with a first embodiment of the invention;

[0017] Fig. 1C is a top view of Fig. 1A, in accordance with a second embodiment of the invention;

[0018] Figs. 2, 3A, 3B, and 4 are sequential cross-sectional views of a substrate undergoing a method of forming the programmable element AF in accordance with a preferred embodiment of the invention;

[0019] Fig. 5 is a top view of the composite antifuse element in accordance with a preferred embodiment of the invention; and

[0020] Fig. 6 is a schematic view of the antifuse circuit in accordance with a preferred of the invention, which includes the composite antifuse element shown in Fig. 5.

Detailed Description of the Invention

[0021] In the invention, the programming energy is decreased by making the fuse elements more susceptible to programming than the other devices on the chip. As such, the programming element can be programmed at the normal chip supply voltage (e.g., Vdd). The invention utilizes a latch that can sense small changes in resistance, such that the "result" of a large

resistance change can be achieved without actually producing a large resistance change.

[0022] Fig. 1A is a cross-sectional view of the programmable element AF of the invention, depicted alongside an FET 31. Isolation structures (not shown in Fig. 1A for ease of illustration) are formed in a substrate 10. Substrate 10 can be either a conventional bulk semiconductor substrate, or a silicon-on-insulator (SOI) substrate. As will be described in more detail below, the AF device has a dielectric 14A that is more susceptible to dielectric breakdown than the dielectric 14B of the FET. This differential is depicted schematically by different thicknesses; as described in more detail below, other techniques of producing this differential in breakdown voltage can be used. Both the antifuse AF and the FET 31 have gate electrodes 16A, 16B, respectively, and sidewall spacers 18. Note that a single diffusion region 20A extends beneath the antifuse AF, and extends towards the FET 31, where the diffusion region 20B provides the source/drain electrodes of FET 31.

[0023] In the invention the dielectric 14A is intentionally fabricated to have a lower breakdown voltage than a normal FET gate dielectric (14B). In practice, the differential in breakdown voltage should be such that upon application of a source voltage Vdd the dielectric 14A breaks down without dielectric 14B breaking down. This result can be achieved in several ways. One way is by thickness; the dielectric 14A is thinner (15-25 angstroms in thickness, in a 0.13 micron CMOS technology) than the dielectric 14B (30-50 angstroms in thickness, in that same technology). These measurements are given in terms of a technology generation for the simple reason that as technologies scale below 0.13 microns, gate dielectrics will become even thinner; in general the 2:1 ratio in respective thicknesses should be maintained, although that differential may decrease with decreasing channel lengths. A feature of the invention is its scalability; because the devices are programmed at the supply voltage, they scale with supply voltage and hence scale with the technology.

[0024] In addition to varying the respective thicknesses of the dielectrics, this differential in breakdown voltage can be achieved by implanting the "weaker" dielectric with ions (such as cesium) that physically damage the film to make it less dense, so as to make it more susceptible to breakdown. Another way would be to implant the dielectric with conductive ions to reduce its insulative value. Or multiple implants could be carried out to achieve both physical damage and conductivity increase. Yet another way would be to provide dopant regions above and/below the dielectric. For example, heavy N+ ions placed above and/or

below the dielectric will enhance the programming field to reduce its insulative value.

[0025] Of these, the option of introducing a variable thickness is most attractive and is thus preferred, simply because it can be best controlled and reproduced in a volume manufacturing environment.

[0026] An embodiment for manufacturing the antifuse of the invention will now be described with reference to Figs. 2-4, which are sequential cross-sectional views of a substrate undergoing the method of the invention. In Figs. 2-4, like reference numerals depict the same elements as those of Fig. 1. In Fig. 2, a dielectric layer 140 is formed on the substrate 10. Layer 140 can be silicon oxide, silicon nitride, silicon oxynitride, multiple layers of one or more of these materials, or other material suitable to serve as a dielectric for the gate electrode of an FET. Moreover, the layer can be formed by growth or deposition (e.g. CVD of oxide in a nitrogen ambient). In the invention, silicon oxide is preferred, formed by thermal growth. Then, a thick layer of silicon nitride 22 (or other material that can be removed selectively to dielectric 140) is coated on the structure.

[0027] In a first alternate embodiment of the method of the invention, as shown in Fig. 3A, a photoresist PR is then applied to the nitride 22, and the nitride 22 is removed down to the underlying dielectric 140. In this alternative, the dielectric 140 that was first grown was the thin oxide 14A (approximately 15 to 25 angstroms in a 0.13 CMOS technology). The opening shown in Fig. 3A is provided in areas where the thicker silicon oxide 14B is to be formed, in this case by growing additional oxide of 15-25 angstroms in thickness.

[0028] In a second alternate embodiment of the method of the invention, as shown in Fig. 3B, the dielectric 140 that is first grown is the thicker oxide 14B. The photoresist PR exposes areas where the thinner oxide 14A is to be formed, and after removal of exposed portions of layer 22 dielectric 14A is formed by etching the thicker oxide. This latter approach is more conducive to some of the other options (ion damage, incorporating a conductor impurity) previously described for introducing a differential in dielectric breakdown voltage between the two dielectrics. For example, either prior to or after completion of this etch process, a first portion of implant 20A is performed under 14A in the silicon area so as to increase the electric field under the fuse. This is also shown in figure 1B. In this embodiment, the electric field enhancement implant 20A, and any subsequent implants used to weaken 14A, would not require an additional masking step.

[0029] In addition to the techniques set forth above, by which oxidations are carried out under normal conditions such that the oxide for the different dielectrics grows at the same rate, this differential in thickness could be provided by carrying out an implants to either retard or enhance oxide growth rates. For example, by implanting a species such as nitrogen prior to gate oxidation, one can alter the oxide thickness in the implanted region to be by 20 to 70 percent thinner than a region not implanted with nitrogen. This is a direct result of retarding the oxidation growth rate. Or, one could enhance the oxidation rate of area 14B relative to 14A by using an oxygen implant in 14B (while masking 14A). Subsequent oxidation would result in a thicker oxide in region 14B relative to 14A.

[0030] Then as shown in Fig 4, the photoresist is removed. If the first alternate embodiment is employed, and the field enhancement 20A or the weakening of the fuse oxide is desired, the following processes would be employed. A photoresist mask covers area 14B and exposes only area 14A, and an implant is carried out to form region 20A as shown in the Figs. This is then followed by removal of all photoresist, and forming a layer of polysilicon that is subsequently planarized on and to the silicon nitride 22, thus forming the individual electrodes 16A and 16A will subsequently become the fuse electrode on 14A, with a field plate 20A both under the electrode, and surrounding it as shown in figure 1B. 16B will become a standard FET gate electrode, surrounded by diffusions 20B that are isolated on each side of 16B by isolation oxide, and are electrically isolated under the electrode 16B by an impurity species of the opposite type as conventionally practiced in the art. The plan view of this structure is depicted in figure 1B.

[0031] Implants can now be performed into the polysilicon, either masked or unmasked (masked is preferred, for control reasons). This process facilitates custom implants to the polysilicon electrodes without affecting the source/drain regions or other portions of the silicon, since they are protected by nitride 22. Implant 1 to the fuse element will be a phosphorous or arsenic implant with a concentration ranging between approximately 5 x 10 e 15 per cm2 (5E15/cm2) and 5E16/cm2, and Implant 2 to the FET gate will be a conventional source/drain implant at a lower concentration than Implant 1. This will locally enhance the applied electric field for the fuse dielectric relative to the dielectric for the FET, enhancing the differential between the two at a given applied gate bias. Note that in general the implants can be of the same dopant and dopant type, or they may be different.

[0032] Note that the implant to form region 20A is masked from all other diffusion implants, and only opened in the region of 16A. The resultant is shown in figure 1B, where 20A becomes continuous around and under 16A by outdiffusion under the spacer 18. Note also that the implant to form region 20B can be carried out through a mask that may either overlap the 20A implant in figure 1B, or it may be carried out through a mask that exposes all of the areas in which 20A and 20B are to be formed. This latter approach assumes the preferred embodiment where the antifuse 16A is n-type gate, region 20A is n-type, and the transistor 31 is an NFET. However, if the transistor 31 is a PFET, and if the junctions 20A and 20B are of a dissimilar type (e.g. 20A is n type, and 20B is p type) then regions 20A and 20B cannot overlap as described in figure 1B. These junctions would be separated by a minimum isolation space 21 as shown in Fig. 1C. The connection in this case between 20A and 20B would be performed at a metal level (versus as in Fig.1B where this connection is a junction connection). The layout of Fig. 1B is superior to the layout shown in Fig. 1C in that the physical structure will be smaller, by the nature of saving an isolation space (large enough to land a metal bridge 23), as well as saving space devoted to the two contacts from 20A and 20B that would be used to connect the junctions an upper metal level. In Fig. 1C, the increased space amounts to the width of space 21 added to the distance between 22 and 18 on both electrodes 16A and 16B, and the distance between 22 to 20A, and the distance between 22 and 20B. The embodiment shown in Fig. 1C has the main advantage of altering the fuse workfunction and junction type (for example N+ electrode 16A and P+ implant 20A) so that the built in potential during programming will be reduced by the workfunction difference of 1.1 volts, thus further enabling a lowered programming voltage.

[0033] Fig. 5 is a top view of the composite antifuse element 200. Note that three antifuse gates 16A, 16A1, 16A2 are disposed parallel to one another within a region that includes the diffusion region 20A. This redundancy helps ensure proper programming - utilizing three fuse elements greatly increases the chances that at least one will have the proper combination of weak dielectric and gate doping to program correctly. The gates are each connected at one end to a respective metal line 28A-28C, and are commonly connected at the other end to a metal line 26. The region 20A receives a voltage via metal line 24. Note that while these connections are referred to as "metal lines," in practice they could be any metal, metal alloy, or doped semiconductor that can provide electrical interconnections.

[0034] Fig 6 is a schematic view of the antifuse circuit 300 which includes the fuse element 200

shown in Fig 5. Metal line 26 of fuse element 200 is coupled to a 10nA current source 35 that charges the fuse element 200 during a read operation through a coupling transistor 36. Metal line 24 of fuse element 200 receives a programming voltage Vp. Metal lines 28A-28C are each coupled to the output of transfer device 36 and to the gate electrode of the FET fuse read transistor 31. The transistor 31 is formed in an isolated well 32 (this well region was not shown in the other Figs. for ease of illustration). The well doping can be controlled to calibrate the off state of the transistor. The drain electrode of the FET 31 is coupled to a voltage source 30, and the source is coupled to a current sense fuse latch 33. The latch 33 can be formed of any combination of transistors that will carry out the operations to be described below; in practice a cross coupled pair of FETS is preferred. The latch 33 is formed in the same well 32 as the transistor 31. The well doping can also be set to precisely control the latch sensitivity (i.e. the latch trip point).

[0035] As will be described in more detail below, when programmed, the antifuse element 200 drives the gate of the read transistor 31, such that the read device off-state (no Ids current) is defined as an un-programmed fuse, and a read device on-state (Ids current flow) is defined as a programmed device. Note that transistor 31 could also be configured as a NFET device, having the property of normally being on (un-programmed state), and off for a programmed device.

[0036] The operation of the antifuse circuit 300 will now be described relative to Fig. 6. Three distinct cycles will be described: read an unprogrammed fuse; program a fuse; and read a programmed fuse. It is to be understood that while two read cycles (unprogrammed and programmed) are described below, in practice a single read cycle is used, the output of which indicates the programmed state of the antifuse element 200.

[0037] A) Read un-programmed fuse:

[0038] 1) Pulse fuse plate 24 to Vp = V1 (normal read voltage. This may in fact be "ground").

[0039] 2) Current source 35 is enabled, charges gate of fuse latch input PFET 31.

[0040] 3) Fuse read device 31 pulsed to V2, and held for the rest of the cycle.

[0041] Result: Fuse gates 16A, 16A1, 16A2 are charged , forcing the PFET 31 to an off state (i.e., a bypass path through the anti-fuse 200 does not exist in the un-programmed state).

[0042] 4) Fuse Latch remains in this initialized state.

[0043] B) Program Fuse:

[0044] 1) Pulse fuse plate 24 to Vp=Vdd. Note that the fuse program level for the thin dielectric is the conventional supply voltage Vdd, which is 1.5-2 volts in a 0.13 technology.

[0045] 2) Transistor 36 is turned off, such that the input 26 to the fuse elements is floating.

[0046] Result: The fuse read device 31 and the current source device 36 do not break down. The Vdd voltage on diffusion 20A causes the gate oxide beneath one or more of the gates 16A, 16A1, 16A2 of the antifuse 200 to break down, producing a low resistance path at the inputs 28A-28C to the antifuse 200. Note that during this time transistor 31 is turned on, causing latch 33 to change state. Thus, a feature of the invention is that programming can be monitored by monitoring the state of latch 33 during program time; if latch 33 changes state, the antifuse element 200 was properly programmed.

[0047] C) Read a Programmed Fuse:

[0048] 1) Pulse fuse plate 24 to Vp = V1

[0049] 2) Current source 35 is enabled, and begins to charge the gate of fuse latch input PFET 31. However, the current path to gate 34 is shunted directly by the programmed fuse element 200 . As a result, fuse latch PMOS transistor 31 turns on. The fuse latch 33 is now changed to a state opposite that of the unprogrammed initialized state.

[0050] Result: The fuse latch 33 is coupled to the fuse programming device 200 via a high impedance network, and the sensing is transformed from a traditional voltage sense means across the fuse element to a current sense having amplification via latch fuse latch PMOS transistor 31.

[0051]

In the above description, fuse read transistor 31 operates as a switch where a programmed or unprogrammed fuse modulates the gate overdrive enough to turn on or cut off transistor 31 completely. In an alternate embodiment, read transistor 31 can be biased as an amplifier with a first source-drain current dependent on an unprogrammed fuse impedance, and a second source-drain current resulting from a change in fuse resistance after programming. With read transistor 31 biased as an amplifier, fuse state can be read as a change in voltage on, or a

change in current through, its drain.

[0052] As set forth above, the antifuse of the invention relies on low programming voltages to set the state of the fuse, due to gate doping and selective gate oxide degradation. An antifuse circuit has been taught that sets a latch as a function of the state of a transistor that operates as a switch or an amplifier, such that the programmed state can be reliably read independent of the actual fuse programmed resistance.

[0053] While the invention has been described above with reference to the preferred embodiments thereof, it is to be understood that the spirit and scope of the invention is not limited thereby. Rather, various modifications may be made to the invention as described above without departing from the overall scope of the invention as described above and as set forth in the several claims appended hereto.